

On page 47, line 2, delete "Figure 8" and substitute

--Figure 8a--.

On page 47, line 5, delete "from left to right" and substitute

-- from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

On page 47, line 9, delete the first "left" and substitute
--right--.

On page 49, line 22, delete "primay" and substitute

--primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figurell" and substitute
--Figure 11--.

On page 60, line 10, after "147" insert --A, B--.

IN THE CLAIMS:

Kindly cancel claims 1-150, without prejudice.

Kindly add the following claims:

1 ~~V-151.~~ A system comprising:

2 a first integrated circuit device coupled to an external
3 signal line, the first integrated circuit device including:
4 output driver circuitry to output data onto the external
5 signal line wherein:

6 the output driver circuitry outputs a first portion of
7 data in response to a rising edge transition of an
8 external clock signal; and

9 the output driver circuitry outputs a second portion
10 of data in response to a falling edge transition of the
11 external clock signal; and

12 a second integrated circuit device coupled to the external
13 signal line, the second integrated circuit device including:

14 output driver circuitry to output data onto the external
15 signal line wherein:

16 the output driver circuitry outputs a first portion of
17 data in response to a rising edge transition of the
18 external clock signal; and

19 the output driver circuitry outputs a second portion
20 of data in response to a falling edge transition of the
21 external clock signal.

1 2 //
2 152. The system of claim 151 further including a clock

3 generator coupled to a second external signal line to generate the
4 external clock signal, wherein the first and second integrated
5 circuit devices are each coupled to the second external signal
line.

3. 153. The system of claim 151 wherein the first and second integrated circuit devices each include a clock alignment circuit coupled to the output driver circuitry.

4 3
1 154. The system of claim 153 wherein each clock alignment
2 circuit is a delay lock loop circuit to generate an internal clock
3 signal, and wherein the output driver circuitry outputs data in
4 response to the internal clock signal.

5 155. The system of claim 151 wherein the first and second
2 integrated circuit devices each further include:

multiplexer circuitry coupled to the output driver circuitry,
wherein:

in response to a first transition of the external clock signal, the multiplexer circuitry couples the first portion of data to an input of the output driver circuitry; and

in response to a second transition of the external clock signal, the multiplexer circuitry couples the second portion of data to the input of the output driver circuitry.

1 156. The system of claim 155 wherein the first and second
2 integrated circuit devices each further include a clock alignment
3 circuit to generate a first internal clock signal, and wherein the
4 multiplexer circuitry couples the first portion of data to the

5 input of the output driver circuitry in response to the first
6 internal clock signal.

1 7 6
2 157. The system of claim 156 wherein the clock alignment
3 circuit generates a second internal clock signal, and wherein the
4 multiplexer circuitry couples the second portion of data to the
5 input of the output driver circuitry in response to the second
internal clock signal.

1 8 1
2 158. The system of claim 151 wherein both the rising edge
3 transition of the external clock signal and the falling edge
4 transition of the external clock signal transpire during a first
clock cycle of the external clock signal.



1 9 1
2 159. The system of claim 151 wherein both the rising and
falling edge transitions of the external clock signal each include
a voltage swing of less than one volt.

1 10 1
2 160. The system of claim 151 wherein the first and second
integrated circuit devices each further include:

3 input receiver circuitry to sample data from the external
4 signal line wherein:

5 the input receiver circuitry samples a first portion
6 of data in response to a rising edge transition of the
7 external clock signal; and

8 the input receiver circuitry samples a second portion
9 of data in response to a falling edge transition of the
10 external clock signal.

1 11. A system comprising:

2 a first integrated circuit device coupled to an external
3 signal line, the first integrated circuit device including:
4 output driver circuitry to output data onto the external
5 signal line wherein:

6 the output driver circuitry outputs a first portion of
7 data synchronously with respect to a rising edge transition
8 of an external clock signal; and

9 the output driver circuitry outputs a second portion of
10 data synchronously with respect to a falling edge transition
11 of the external clock signal; and

12 a second integrated circuit device coupled to the external
13 signal line, the second integrated circuit device including:

14 input receiver circuitry to sample data from the external
15 signal line wherein:

16 the input receiver circuitry samples the first portion
17 of data synchronously with respect to the rising edge
18 transition of the external clock signal; and

19 the input receiver circuitry samples the second
20 portion of data synchronously with respect to the falling
21 edge transition of the external clock signal.

1 12 11
162. The system of claim 161 further including a clock
2 generator coupled to a second external signal line to generate the
3 external clock signal, wherein the first and second integrated
4 circuit devices receive the external clock signal.

1 13 11
163. The system of claim 161 wherein the first integrated
2 circuit device further includes a clock alignment circuit to
3 receive the external clock signal and to generate an internal clock
4 signal, wherein the output driver circuitry outputs data in
 response to the internal clock signal.

1 14 11
164. The system of claim 161 wherein the first integrated
2 circuit device further includes:

3 multiplexer circuitry coupled to the output driver circuitry,
4 wherein:

5 in response to a first transition of the external clock
6 signal, the multiplexer circuitry couples the first portion of
7 data to an input of the output driver circuitry; and

8 in response to a second transition of the external clock
9 signal, the multiplexer circuitry couples the second portion
10 of data to the input of the output driver circuitry.

1 15 165. The system of claim ~~161~~ wherein both the rising edge
2 transition of the external clock signal and the falling edge
3 transition of the external clock signal transpire during a first
4 clock cycle of the external clock signal.

1 166. The system of claim ~~161~~ wherein both the rising and
2 falling edge transitions of the external clock signal include
3 voltage swings of less than one volt.

1 17! 167. The system of claim ~~161~~ wherein the second integrated
2 circuit further includes a clock alignment circuit to receive the
3 external clock signal and to generate an internal clock signal,
4 wherein the input receiver circuitry on the second integrated
5 circuit device samples data in response to the internal clock
6 signal.

Just B1 168. An integrated circuit device comprising:

2 output driver circuitry to output data onto a first external
3 signal line wherein:

4 the output driver circuitry outputs a first portion of
5 data in response to a rising edge transition of a first
6 external clock signal and the output driver circuitry outputs
7 a second portion of data in response to a falling edge
8 ~~transition of the first external clock signal.~~

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169. The integrated circuit device of claim ~~168~~ further
including input receiver circuitry to sample data from a second
external signal line wherein:

the input receiver circuitry samples a first portion
of data in response to a rising edge transition of a
second external clock signal; and

the input receiver circuitry samples a second portion
of data in response to a falling edge transition of the
second external clock signal.

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device 19

C 1 ~~170.~~ The integrated circuit of claim ~~169~~ further including
2 a clock alignment circuit to generate a first internal clock
3 signal, and wherein the input receiver circuitry samples the first
4 portion of data in response to the first internal clock signal.

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1 171. The ~~system~~ of claim 170 wherein the clock alignment
2 circuit generates a second internal clock signal, and the input
3 receiver samples the second portion of data in response to the
4 second internal clock signal.

first
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1 172. The integrated circuit device of claim 168 wherein the
2 clock alignment circuit generates an internal clock signal, and the
3 output driver circuitry outputs data in response to the internal
4 clock signal.

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1 173. The integrated circuit device of claim 168 further
2 including input receiver circuitry to sample data from the first
3 external signal line wherein:

4 the input receiver circuitry samples a first portion of
5 data in response to a rising edge transition of the first
6 external clock signal; and

7 the input receiver circuitry samples a second portion
8 of data in response to a falling edge transition of the first
9 external clock signal.

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1 174. The integrated circuit device of claim 168 further
2 including:
3 multiplexer circuitry coupled to the *first* output driver circuitry,
4 wherein:

5 in response to a first transition of the first
6 external clock signal, the multiplexer circuitry couples the
7 first portion of data to an input of the ^{first}
8 output driver
circuitry; and

9 in response to a second transition of the first
10 external clock signal, the multiplexer circuitry couples the
11 second portion of data to the input of the ^{first}
12 output driver
circuitry.

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1 175. The integrated circuit device of claim ~~174~~ further
2 including a clock alignment circuit to generate a first internal
3 clock signal using the first external clock signal, wherein the
4 multiplexer circuitry couples the first portion of data to the
5 input of the ^{first}
6 output driver circuitry in response to the first
7 internal clock signal.

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1 26
2 176. The integrated circuit device of claim ~~175~~ wherein the
3 clock alignment circuit generates a second internal clock signal,
4 and wherein the multiplexer circuitry couples the second portion of
5 data to the input of the ^{first}
6 output driver circuitry in response to the
7 second internal clock signal.

1 27
2 B3
3 177. The integrated circuit device of claim 176 further
4 including a clock alignment circuit coupled to the first external